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MODEL PCI-WDG-CSM

USER MANUAL

FILE: MPCI-WDG-CSM.F1d

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Table of Contents

Chapter 1: Introduction

This multifunction card contains a watchdog timer. Additionally, one or more options may be included on your card. These are: a computer power supply monitor, a computer internal temperature monitor, capability to read the temperature, pair of opto-isolated inputs and outputs, a fan-speed control, and an on-card alarm to signal watchdog timeout.

Watchdog

Your application program must communicate with the watchdog circuit at prescribed intervals. If this communication ("prompt") is missed, the Watchdog can be programmed to initiate a computer reset (reboot). If the reboot is successful, operation may be returned to the previous application program. If the failure was temporary, proper operation is resumed. If, however, the failure is persistent, the Watchdog will continuously reset the computer. The more frequently the Watchdog is prompted (and shorter Watchdog time selected), the less time a faulty computer has to cause damage.

The method used by the card to detect loss of computer function is as follows:

A type 82C54 counter/timer is used. This chip contains three 16-bit counters. A number greater than zero is set into the chip's Counters by your application program. The Watchdog is armed by software command and the counters begin counting down. As long as the computer is operating properly, the counters will be periodically reloaded to their original programmed values by your application program before the counters have counted down to zero. (See Chapter 5, Programming, Foreground Watchdog Mode, or Background Watchdog Mode for detailed information.)

If your software fails to reload the counters, then both counters continue counting until zero is reached (timeout). When the counters 0 and 1 reach zero, the reset or power-good line is held low performing a hardware reset through a relay contact, open collector transistor, or a de-bounced opto-isolated switch while the optional on-board buzzer alarm sounds (if enabled). When a reset condition occurs, the reset circuit is active until a reset pulse returns from the system bus or power is cycled to the system, or counter 2 times out.

The clock frequency to Counter 0 is derived from the computer's clock and is

33 MHZ÷16= 2.08333 MHz. (The period is 0.48 µsec.)

The output of Counter 0 is used as a clock to Counter 1. Each counter can divide by any whole number from 2 to 65,536 (2^{16}), so the watchdog timeout period may vary from about 2 microseconds to 2060 seconds.

The duration of the watchdog reset output (WDRST) and ("not WDRST") can be programmed at Counter 2. There are two clock rates available for the counter and you can select the rate that best suits your needs. The default clock rate is half the PCI bus clock speed, 16.67 MHz. You can select a lower rate (2.08333 MHz) by a write to base address+C. That selection will be held until a read to base address +C.

The watchdog card can generate an interrupt request one Counter 0 period-width before the reset timeout. For example, if a reset period of 60 seconds is used with a 5 millisecond delay stored in Counter 0 (the result of a maximum value delay), an interrupt would occur at 59.995 seconds. This gives the Interrupt handler software 5 milliseconds to refresh the watchdog before a reset action occurs. This should allow your software to take corrective actions if the system software continued to run but the software that should have reset the watchdog had failed. Discussion of these Watchdog Programming Options is given in a later chapter.

There are several inputs and outputs from the card: (See Chapter 6 for pinout.)

a. Double-pole double-throw, Form C, relay contacts on the rear panel I/O connector.
b. An opto-isolated reset output on the rear panel I/O connector.
c. An opto-isolated complement of the reset output on the rear panel I/O connector.
d. A buffered TTL CTRGATE (counter enabled) output on the rear panel I/O connector.
e. TTL Reset signal (active high) on internal terminal block.
f. Open collector Reset signal (active low) on internal terminal block.
g. A Watchdog 130.208KHz "heartbeat" on the rear panel I/O connector.
h. Un-fused 5V DC output at the rear panel I/O connector.
i. Fan Drive Power return on internal terminal block.
j. Fan Drive Power out on internal terminal block.
k. "Fan Reset" can initiate a fan restart if the fan stops. (pulled down, requires a momentary high signal to initiate a fan restart)

As noted in items b. and c. above, opto-coupled outputs (one ON when the other is OFF) are provided for use where relay contact bounce could be a problem. Further, as noted in e. above, a buffered discrete output is also provided. This output goes high to signal a watchdog reset condition. Finally, a 130.208 kHz, TTL-level, 50 percent duty cycle signal is provided at I/O connector pin 13 when the watchdog circuit is enabled and no reset is in progress. Otherwise, this output is in a low state.

Options

Your card may have one or more options installed as mentioned in the opening paragraph of this description. The following paragraphs describe these options.

Option 01: Computer Power Monitor
The three computer power supplies (+5V, +12V, and -12V) are monitored. If one or more of those voltages are more than +6% outside of their nominal values, then two bits of a Status Register indicate whether there is an overvoltage or an undervoltage. In addition, an interrupt request can be generated.

Option 02: Computer Temperature Monitor
If this option is installed, Option 01 must also be installed. This option monitors ambient temperature inside the computer chassis. The temperature monitor circuit compares the output of an LM334 temperature sensor with a preset DC voltage level. The output of the circuit can be read at a bit location of the Status Register and, also, can cause an interrupt request if that temperature exceeds the factory preset limit (50 °C).

Option 03: Computer Temperature Measurement
This option requires presence of both Option 01 and 02. When this option is included, an onboard 8 bit A/D converter provides means for a software read of the measured temperature. Resolution is to approx. 0.7 °F.

Option 04: This Option Provides Three Functions as Follows:

Change of State
Differential digital inputs are accepted through pins 17 & 18 (ISOIN0) and pins 19 & 20 (ISOIN1), are opto-isolated and reported in the Status Register. The change-of-state also generates an IRQ interrupt request. User must supply current limiting bias resistor in external circuitry (Example: Connect +5V through a 470 ohm or, connect 24V through a 2.2K ohm resistor to the Anode, with the Cathode connected to an active low TTL output for control.)

Buzzer
The buzzer is under software control and can be turned on by programming a "write" to Base Address + 4 or off by programming a "write" to Base Address +5 or if enabled, the buzzer will turn on during watchdog reset.

Opto-Isolated Outputs
This option provides an opto-isolated reset signal at pins 4 and 5 (Isolated Reset Output) of the DB25 connector. An opto-isolated inverse of the reset signal is also provided across pins 6 and 7 (Isolated NOT Reset Output) of the same connector. User must supply source voltage and load resistor in external circuitry. (Example: Connect +VCC to the Collector and a 1K ohm resistor (load) from Ground to the Emitter. This gives you a non-inverting output by tying to the Emitter. For an inverting output, connect a 1K ohm resistor from the +VCC to the Collector, and the line to be controlled to the Collector below the load resistor, and ground the emitter.)

Option 05
This option deletes the opto-isolated Reset output capability and replaces it with capability to provide outputs under computer control. When this option is installed, both of these outputs are computer controlled. To activate the Opto-Isolated Reset output, a write to base address+D is required, to deactivate a read to base address +D is required. To activate the Opto-Isolated NOT reset, a write to base address+E is required. To deactivate a read to base address +E is required. Both of these outputs are deactivated by a computer reset.

Option 06
When this option is installed it is used in conjunction with Option 02 to maintain internal temperature in the computer by the control of fan speed. The duty cycle of fan power (+12V) is pulse-width modulated to speed up the fan when temperature increases. If no current is detected or the duty cycle reaches 100 percent, an interrupt occurs.

Special Options
Programmable array logic is available on this card and many possibilities exist for special modifications to suit unique requirements. If your card includes any such modifications, there will be an "Addendum" sheet inserted at the front of this manual and an "S" number (e.g. S08, S09, etc) will be appended to the model number.

Status Register

Bit assignments of the Status Register are as follows:

BD0	Watchdog counter refresh reminder (Active low)
BD1	Temperature good (Active high)
BD2	Isolated Input #0 status (Same as input)
BD3	Isolated Input #1 status (Same as input)
BD4	Fan good (Active high)
BD5	Power Supply overvoltage (Active low)
BD6	Power Supply undervoltage (Active low)
BD7	IRQ generated (Active high)

Specification

Watchdog Timer

- Time-out: Software selectable from 2 µsec. to 2060 sec
- Output Pulse Width: 120 nsec. Minimum, 31 msec. Maximum
- Clock: 2.08333 MHz, derived from computer clock (33 MHz÷16)
- Address: Continuously mappable within 0000 to FFFF hex I/O range
- Relay Output: DPDT, Form C, max. switching current 2A DCat 30W or 1.25A AC at 30VA max
- Open Collector Output: /WDRST Active low, 200mA sink max
- TTL Output: WDRST source 15mA @ 3.1V typical, sink 64mA @ 0.4V typical
- Interrupt Output: PCI-INTA

Status Monitor Options

- Voltages IRQ and status register indication if +5, +12, or -12 V exceed +/- 6% of nominal
- Temp. Alarm: IRQ and status register indication at 122 °F. and above
- Temp. Sensor: 8 bit ADC, LSB = 0.7 °F. (factory adjustable)
- Buzzer: Audio Alert signals watchdog timeout
- LED Output: 5V, through a 470 Ω resistor
- Isolated Inputs: Two, opto-isolated, 10 mA typical bias, 60mA max
- Isolated Outputs: Complimentary opto-isolated reset outputs (2). 5mA typical load @ 30Vmax, 30mA maximum
- Fan Speed: IRQ and Status Register indication whenever speed is out of range

Environmental

- Operating Temperature Range: 0 °C. to +60 °C
- Storage Temperature Range: -50 °C. to +120 °C
- Humidity: 10% to 90% RH, non-condensing
- Power Required: +5 VDC at 125 mA w/ no options, 250 mA all options installed
- Size: 6.7 inches long (170 mm) x 3.9 inches high (99 mm)

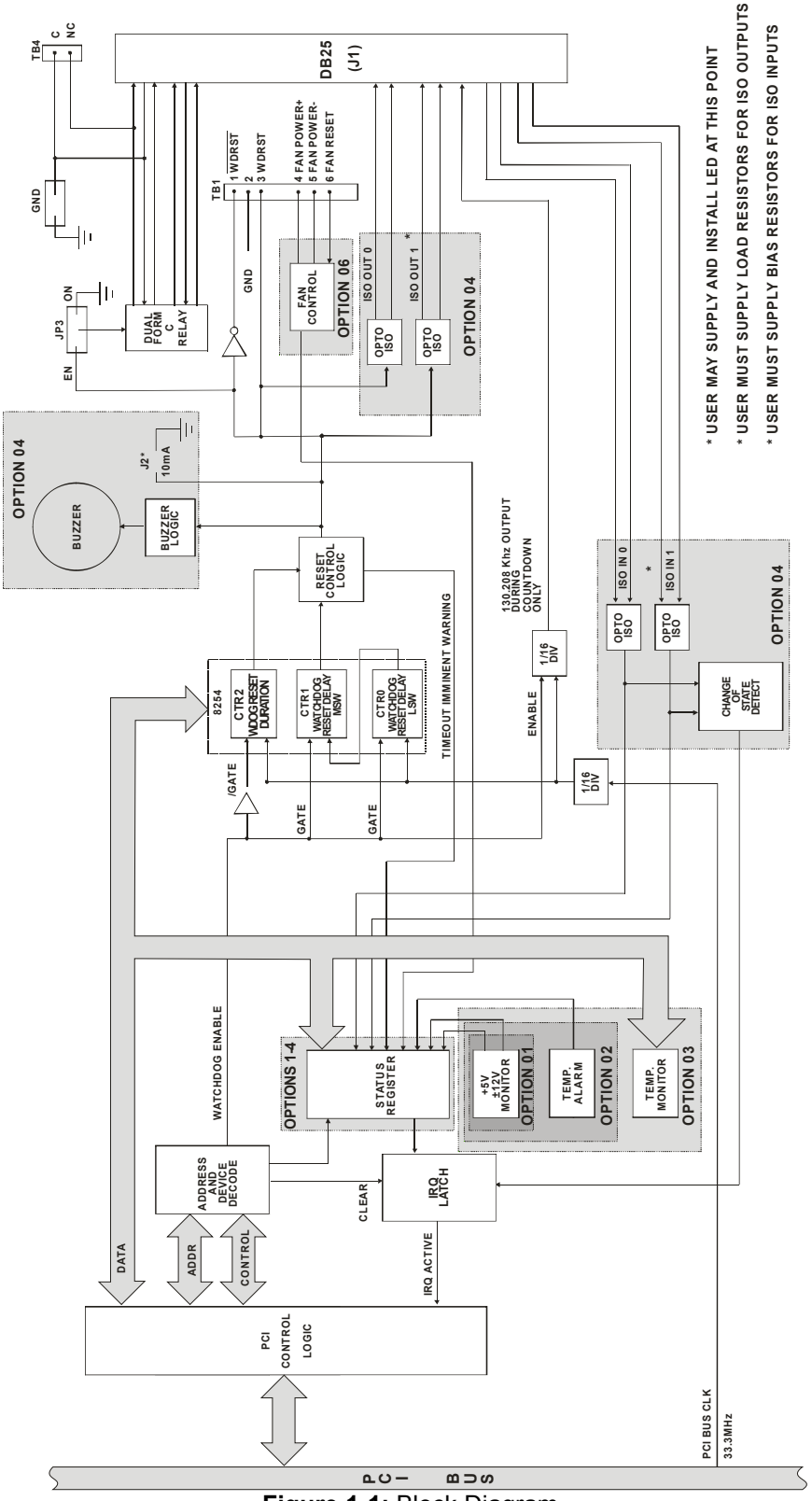


Figure 1-1: Block Diagram

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the card for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this card is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system.

Configure Card Options via Jumper Selection

Before installing the card into your computer, carefully read Chapter 3: Option Selection of this manual, then configure the card according to your requirements. Our Windows based setup program can be used in conjunction with Chapter 3 to assist in configuring jumpers on the card, as well as provide additional descriptions for usage of the various card options.

CD Software Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Caution! * ESD A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETUP.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Carefully install the card in an available 5V or 3.3V PCI expansion slot (you may need to remove a backplate first).
6. Inspect for proper fit of the card and tighten screws. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7. Install an I/O cable onto the card's bracket mounted connector.
8. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
9. Run PCIfind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
10. Run one of the provided sample programs that was copied to the newly created card directory (from the CD) to test and validate your installation.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck PCIFind or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In DOS, the PCI\SOURCE directory shows the BIOS calls used to determine the address and IRQ assigned to installed PCI devices. In Windows, the Windows sample programs demonstrate querying the registry entries (created by PCIFind and NTIOPCI.SYS during boot-up) to determine this same information.

Input/Output Connections

Connections are made via a 25-pin FEMALE connector on the card mounting bracket. Also, there are either one or two, three-terminal blocks, and one four pin header for connecting to the reset line or power good line, or other functions, depending on the options purchased. Signal assignments are listed in Chapter 6 of this manual.

To ensure that there is minimum susceptibility to EMI and minimum radiation, it is important that the card mounting bracket be properly screwed into place and that there be a positive chassis ground. Also, proper EMI cabling techniques (cable connect to chassis ground at the aperture, shielded twisted-pair wiring, etc) be used for the input/output wiring.

Connecting the Reset Line
If your computer is equipped with a reset button you must connect reset button wires across the “C” and “NC” header at the top rear edge of the Watchdog card as shown in figure 2-1. Install the “ON/EN” jumper on the Watchdog card in the “EN” position. Then using the cable connect the second set of “C” and “NC” header pins to the Reset pins on the mother board. The hot side of this connection must be connected on the “NC” side of the header. You can determine which reset push button wire is hot by removing the reset pushbutton connector from the motherboard and measuring for +5VDC on the pins. Alternatively, you can try to connect into one wire, running the sample program, and if it doesn't work, try connecting to the other wire.

If there is no reset push button and your computer is equipped with an ATX power supply, connect the power good line to the “NC” header pins on the Watchdog card as shown in figure 2-2. To make a connection, insert the cable into the clamp, compress the metal bar with pliers and close the protective cover. Install the “ON/EN” jumper on the Watchdog card in the “EN” position. Then install a jumper on the “GND” header on the Watchdog card.

If there is no reset push button and your computer is equipped with an AT-type power supply, you can connect the power good line on P8 of the Mother Board to the /WDRST terminal of the watchdog card as shown in figure 2-3, or connect the power good line to the “NC” header as shown in figure 2-2. Note: If the “NC” header is used ensure that a jumper is installed on the “GND” and the “EN” headers on the Watchdog card.

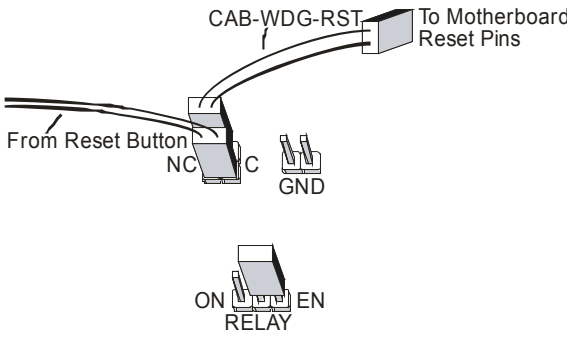


Figure 2-1: Reset Button Connection

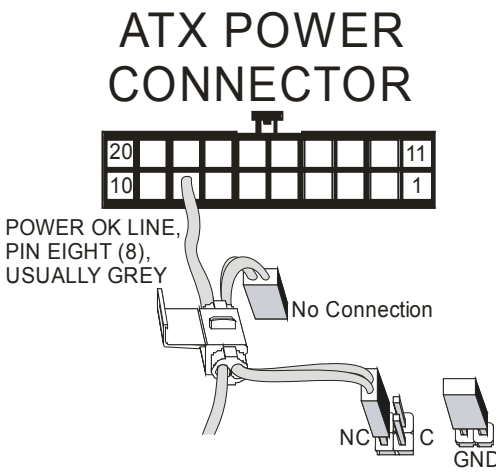


Figure 2-2: ATX Power Good Connection

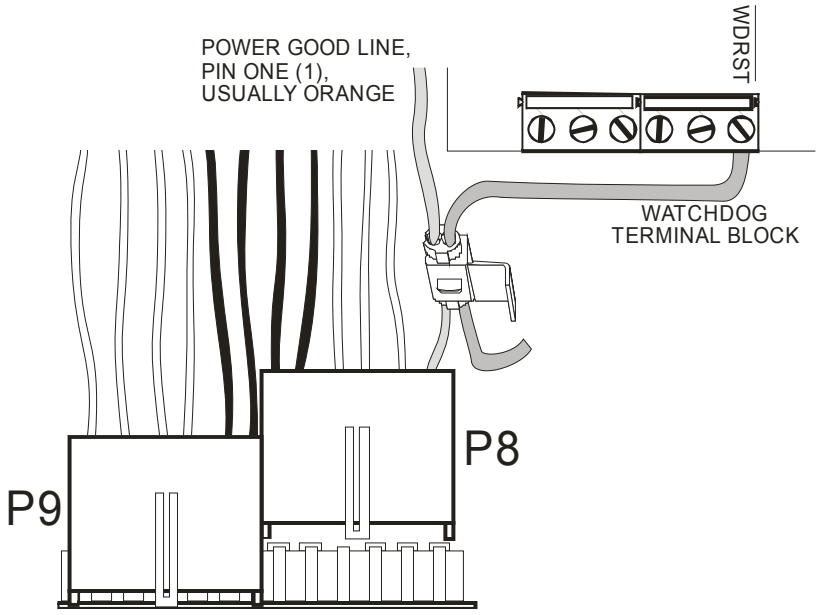


Figure 2-3: AT Power Good Connection

Connecting a Fan

If you purchased a card with Option 6, Fan Speed Control, your card will be populated with six screw terminals at the back end, opposite side from the mounting bracket and DB25 connector. The bottom three terminals are associated with your fan connection. The minimum required connections are the black and red or yellow wires connected to FAN + and FAN -. In the case of a three wire fan, remove the black and red or yellow wires from the connector body and insert them (black to black FAN – and yellow or red to FAN +) into the screw terminals then tighten the screw onto the crimp. The green wire should be left in the 3-pin connector body that you unplugged from the motherboard, then plug that connector back onto the motherboard. To use the bottom “FAN RESET” terminal connect a momentary dry contact switch across this terminal to the FAN + terminal. To restart a fan that has stopped, push the momentary switch which should signal the fan controller chip on our card to switch the status bit to FAN GOOD, which should then restart the fan.

Chapter 3: Option Selection

Refer to Figure 1-1, Block Diagram and Figure 3-1, Option Selection Map when reading this section of the manual. Card operation is determined by jumper installation as described in the following paragraphs.

Relay Enable/Disable

Hold the card with the fingers at the bottom and the mounting bracket on the left. The relay-control jumper is located alongside the relay at the left-hand side of the card. If no jumper is placed on the block, the relay is always de-energized. If a jumper is placed between the two left-hand posts, the relay is always energized when +5V power is on. If a jumper is placed between the two right-hand posts, the relay is de-energized during reset (watchdog timeout), and the relay is energized on powerup. If you desire to use the relay output, then the jumper should be placed between the right-hand posts.

Screw Terminals

Screw terminals located on the right-hand side of the card provide the means for connections of the watchdog output to points inside the computer chassis. The top terminal provides the active-low watchdog output. The next terminal provides a ground. The third terminal provides the complementary active-high of the first terminal output. The fourth terminal down provides power to the computer fan and the fifth terminal from the top provides pulse-width modulated control for fan speed. The bottom terminal is an input that can re-start the fan.

ATX/Reset Button Header

For ATX supplies, the top left-hand side of the card has a four pin header to provide a ground to reset the computer through a relay contact (same contacts on 25 pin I/O connector, pins 14 Common, and 15 NC). Use the NC terminal with the “GND” jumper installed to apply a ground through the jumper and relay contacts, then to the power good or reset line. This connection can alternately be connected to the reset button pins on the mother board. The GND jumper must be removed if the reset button connection is used. Upon boot up, the relay becomes energized.

LED Terminals

A connector for an external or on-board LED is provided at two solder pads labeled J2. The output is limited by a 470 ohm resistor in series with a 5V output. This output is only active if the Buzzer option is installed.

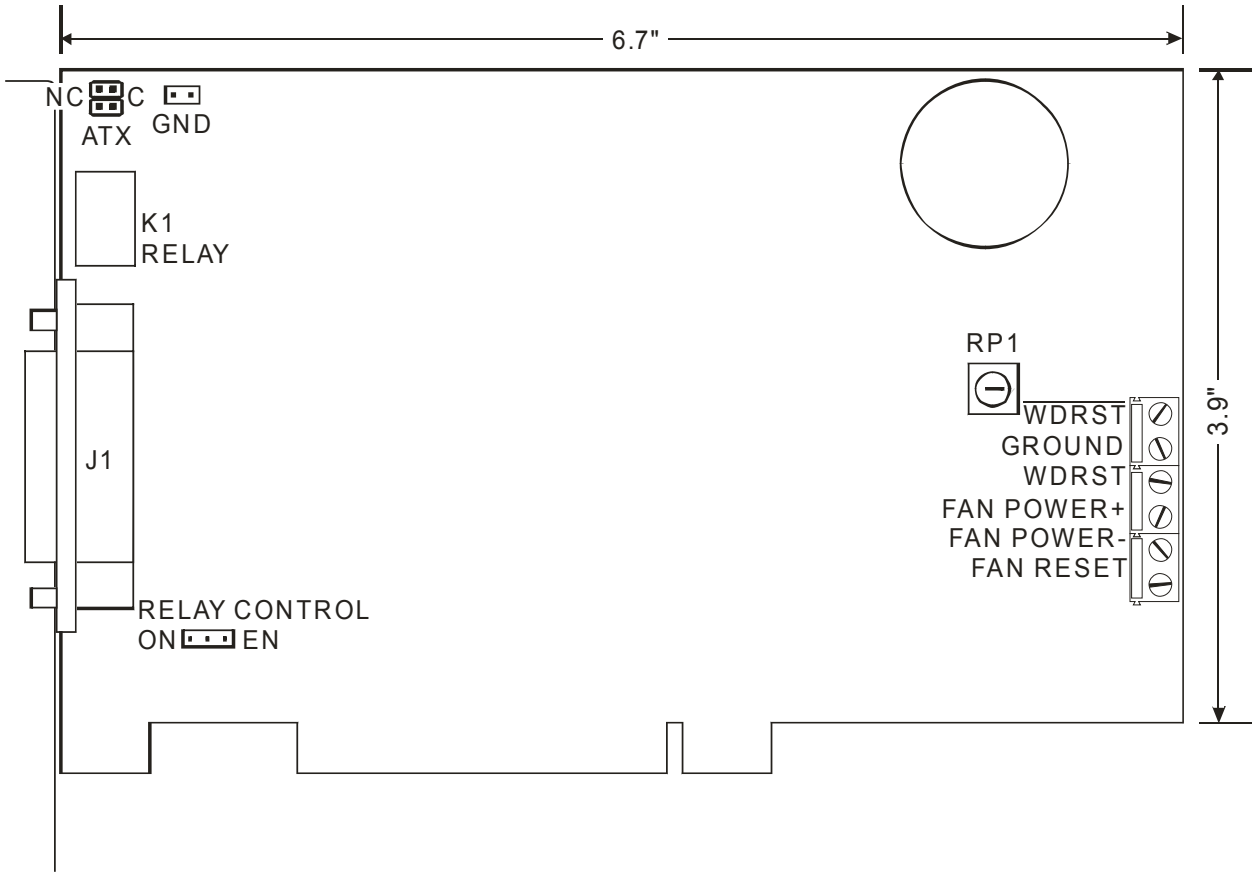


Figure 3-1: Option Selection

Chapter 4: Address Selection

The card uses one PCI address space, occupying 16 consecutive register locations.

PCI architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCI cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, Windows systems can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind, or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

The PCI bus supports 64K of address space, so your card's addresses may be located anywhere in the 0000 to FFFF hex range.

PCIFind uses the Vendor ID and Device ID to search for your card, then reads the base address and IRQ.

To determine the base address and IRQ yourself, use the following information.

The Vendor ID for the card is 494F. (ASCII for "IO")
The Device ID for the card is 22C0h.

Chapter 5: Programming

This section of the manual contains information to assist you in developing programs for use with the card. I/O bus address assignments, programming hints, and a description of the utility driver are included.

Monitor Functions

The card uses sixteen consecutive registers in I/O space as listed in the following table

Address	Read	Write
Base Address	Read Counter #0	Write to Counter #0
Base Address +1	Read Counter #1	Write to Counter #1
Base Address +2	Read Counter #2	Write to Counter #2
Base Address +3	Read Control Register	Write to Control Register
Base Address +4	Read Status Register, Clear IRQ, Enable IRQs	Start Buzzer (if enabled)
Base Address +5	Read Temperature	Stop Buzzer
Base Address +6	Disable Buzzer	Enable Buzzer
Base Address +7	Disable Counters	Enable Counters
Base Address +8	Unused	Unused
Base Address +9	Unused	Unused
Base Address +C	Hi Rate Clock Select	Low Rate Clock Select
Base Address +D	Disable Opto-Output NWDRST	Enable Opto-Output NWDRST
Base Address +E	Disable Opto-Output WDRST	Enable Opto-Output WDRST
Base Address +F	Unused	Unused

Table 5-1: Register Address Map

Computer Temperature Monitor

If Option 03 is installed, the temperature inside the computer can be read using an 8-bit register at BASE+5. To convert the byte read into temperature in Fahrenheit, multiply the value read by 11/15 and then add 7.

Interrupts

Interrupts are disabled at power-up to prevent an interrupt during boot-up. Interrupts are enabled by a read of the Status Register at BASE+4, and disabled by a read of the Status Register at BASE+9. Pending interrupts are cleared by a read of either of these registers, or the Status Register at BASE+8. The card is capable of generating interrupts for a variety of reasons. If any or all of the standard options described on page 2-3 are installed (as well as the watchdog-timeout-near warning), they can be read from the Status Register at BASE+4. Bit assignments are as listed on the following page. An interrupt is also generated upon a digital input's change-of-state if that option is installed.

Status Register

Bit assignments of the Status Register (Base Address +4) are as follows:

BD0	Watchdog counter refresh reminder (Active low)
BD1	Temperature good (Active high)
BD2	Isolated Input #1 status (Same as input)
BD3	Isolated Input #0 status (Same as input)
BD4	Fan good (Active high)
BD5	Power Supply overvoltage (Active low)
BD6	Power Supply undervoltage (Active low)
BD7	IRQ generated (Active high)

Watchdog Programming Options

Programming the card is straightforward. Counters 0 and 1 of the type 8254 counter/timer are concatenated and operate as a 32-bit down counter to provide the time delay before a timeout occurs. A special register provides enable and disable functions for the counters and, thus, the watchdog itself. Writing any value to the register located at base address +7 enables the counters to count. Reading the register disables the counters and stops the watchdog.

To Program the Watchdog Interval

1. Disable the counters.
2. Program the counters with the desired time delays.
3. Enable the counters.

Once the counters have been enabled, the computer will reset if the 32-bit counter decrements all the way to zero. (Note: An alternative use of the reset signal is to simply notify an external device that a reset is necessary.)

Foreground Watchdog Mode

In order to prevent the reset, the software program must periodically reload the Counter 1 with the initial load value (or any other suitable load value). The maximum delay between Counter 1 reloads is determined by the load values of the concatenated counters minus a suitable fudge factor. (Note: It is not necessary to re-load Counter 0 because it will simply recycle. Also note that loading Counter 0 with full-scale is customary, as exact timing is rarely a requirement of a watchdog function.)

Counter 0 must be programmed for mode 3. Counter 1 and 2 must be programmed for mode 2. The card was designed specifically for these modes. Any other modes may cause unpredictable behavior. See Appendix A for details on how to program the counters.

In Summary:

1.	Disable Watchdog	Read BASE+7
2.	Program CTR0 for Mode 3	See Appendix A
3.	Program CTR1 and 2 for Mode 2	See Appendix A
4.	Load CTR0,1,2 with reset delay	See Appendix A
5.	Enable Watchdog	Write BASE+7

Then, before the first timeout occurs:

1.	Enter main loop	
2.	Program CTR1 (again) for Mode 2	
3.	Load CTR1	See Appendix A
4.	User code goes here	
5.	Repeat main program loop	

Background Watchdog Mode

An alternative method to refresh the counters that provides some flexibility but potentially reduces dependability is to use an interrupt service routine (ISR). The card will generate an interrupt one Counter 0 load value before timeout occurs. If that interrupt is used by a user-defined ISR, it's possible for that ISR to refresh the counters and, thus, avoid need for the main program loop to refresh the counters.

There is possibility of reduced dependability because this method will not detect certain types of program lock-ups. For example, if the application program were to lock up in a loop such as "JMP $", the interrupt service routine would never know it and would therefore continue refreshes despite the lockup. It is possible to modify the host program to enable the ISR to detect such loops (perhaps by checking the return stack location for the ISR each time, and making sure it changes...) However, if the code is going to be modified, the next, hybrid, method might be more effective.

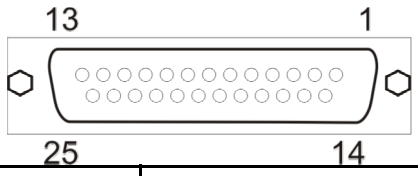
This method does, however, allow "off-the-shelf" existing programs to be used with the card without modification. Also, this method could cause spurious resets if your program disables interrupts for an extended duration. The IRQ that would have caused the ISR might be missed and allow the counter to time out. If the counter counts-down, the reset signals will be generated and the counters will restart.

Combination Reset Mode

By combining the two methods ("Foreground" and "Background") it is possible to create a very elaborate scheme for monitoring the status of the computer. This combined method eliminates the negatives associated with either method used individually, but does require extensive modifications to existing code, or even rewriting code entirely. In this scheme, both foreground and background routines can prompt the watchdog.

The foreground routine would prompt the watchdog under normal conditions, and the ISR running in the background would only prompt the watchdog if the foreground routine failed to do so. The ISR, noting that the foreground routine missed its prompt, could take steps to determine why, and even try to correct it. For example, the foreground program can post its current status to a shared-memory variable, indicating that it is about to enter a long dedicated process (calculations for a print job, perhaps) and that it might miss several of its prompts. The ISR, when executed by the warning IRQ, notes that the foreground program indicated it might miss its turn, and starts counting misses. After prompting the watchdog, it returns control to the foreground process. If the count of missed prompts gets too high, it could write status to a disk file or serial port, then skip the prompt, allowing the computer to reset.

Chapter 6: Connector Pin Assignments



DB-25 Female

Pin Number	Function
1	Relay Pole 1, Common Contact (C)
2	Relay Pole 1, Normally Closed Contact (NC)
3	Relay Pole 1, Normally Open Contact, (NO)
4	Opto-Isolated Output Emitter (WDRST or Output 0)
5	Opto-Isolated Output Collector (WDRST or Output 0)
6	Opto-Isolated Output Collector (NWDRST or Output 1)
7	Opto-Isolated Output Emitter (NWDRST or Output 1)
8	Watchdog Counter Enabled (Output)
9	+5 VDC Unfused, 1A max
10	+5 VDC Unfused, 1A max
11	+5 VDC Unfused, 1A max
12	+5 VDC Unfused, 1A max
13	130.2 KHz Square Wave while the Watchdog is enabled
14	Relay Pole 2, Common Contact (C)
15	Relay Pole 2, Normally Closed Contact (NC)
16	Relay Pole 2, Normally Open Contact (NO)
17	Opto-Isolated Input #0 Source (Anode)
18	Opto-Isolated Input #0 Return (Cathode)
19	Opto-Isolated Input #1 Return (Cathode)
20	Opto-Isolated Input #1 Source (Anode)
21	Fan Restart Input (pulled down, active high)
22	Ground
23	Ground
24	Ground
25	Ground

Table 6-1: DB25F Connector J1 Pin Assignments

Top Terminal	/WDRST	Open Collector Watchdog Output - Active Low
2nd Terminal	GROUND	Ground, General Purpose
3rd Terminal	WDRST	TTL Watchdog Output - Active High
4th Terminal	FAN + (RED)	+12V (Fan Red or Yellow Wire)
5th Terminal	FAN – (BLACK)	Open Collector PWM (Fan Black Wire)
Bottom Terminal	FAN RESET	Fan Restart Input - Active High (See Pin 21 - Connector)

Table 6-2: On-Board Terminal Block Pin Assignments

Appendix A: Programmable Interval Timer

This Appendix includes basic information about the type 8254 Counter/Timer chip. For those interested in more detailed information, a full description can be found in the manufacturer's data sheets.

Please note: The information in this Appendix is for general reference, and may include features or functions not applicable to this card.

Operation Modes

Modes of operation are described in the following paragraphs to familiarize you with the power and versatility of this device. The following conventions apply in describing operation of type 8254 chips:

Clock:	A positive pulse into the counter's clock input.
Trigger:	A rising edge input to the counter's gate input.
Counter Loading:	Programming a binary count into the counter.

Mode 0: Pulse on Terminal Count
After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing. This mode is commonly used for event counting with Counter #0.

Mode 1: Retriggerable One-Shot
The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. Thus, this forms a re-triggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator
This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low. This mode also works well as an alternative to mode 0 for event counting.

Mode 3: Square Wave Generator
Like mode 2, this mode operates periodically. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that, in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the waveform.

Mode 4: Software Triggered Strobe
This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe
In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will go low until the full count after the rising edge of the trigger.

Programming

On the card, the 8254 counters occupy the following addresses:

Base Address	Read/Write Counter 0
Base Address +1	Read/Write Counter 1
Base Address +2	Read/Write Counter 2
Base Address +3	Read/Write Counter Control Register

The counters are programmed by writing a control byte into the counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is a follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0 and SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter 0
0	1	Program Counter 1
1	0	Program Counter 2
1	1	Read/Write Command

RW0 and RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0, M1, and M2: These bits set the operational mode of the selected counter.

Mode	M2	M1	M0
0	0	0	0
1	0	0	1
2	x	1	0
3	x	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (0) or BCD (1).

Reading and Loading the Counters

If you attempt to read the counters on the fly when there is a high frequency input, you will most likely get erroneous data. This is partly caused by "carries" rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it's possible that "carries" will be propagated from the low byte to the high byte during the read cycle.

To circumvent this, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW0 and RW1 bits with zeroes. This instantly latches the count of the selected counter in a 16-bit hold register. (An alternative method of latching counters that has an additional advantage of operating simultaneously on several counters is by use of a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading, by bringing the gate low, or by halting the input pulses.

You must specify in advance the type of read or write operation that you intend to perform for each counter. You have a choice of loading/reading (a) the high byte of the count, (b) the low byte of the count, or (c) the high byte followed by the low byte. This last is of the most general use and is selected for each counter by setting the RW0 and RW1 bits to ones. Of course, subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step.
The readback command byte format is:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	CNT	STA	C2	C1	C0	0

CNT: When is 0, latches the counters selected by bits C0-C2.
STA: When is 0, returns the status byte of counters selected by C0-C2
C0,C1,C2: When high, select a particular counter for readback. C0 selects Counter 0, C1 selects counter 1, and C2 selects counter 2.

You can perform two types of readback operations with the readback command. When CNR=0, the counters selected by C0-C2 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT:Current state of counter output pin.
NC: Null count. this indicates when the last count loaded into the counter register has actually been loaded into the counter itself. The exact time of load depends on the configuration selected. Until the count is loaded into the counter itself, it cannot be read.

RW0 and RW1: Read/Write command.
M0-M2: Counter mode.
BCD: BCD=0 sets binary mode, otherwise counter is in BCD mode.

If STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a counter address location will yield:

1st Read:	Status byte
2nd Read:	Low byte of latched data
3rd Read:	High byte of latched data.

After any latching operation of a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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