ACCES I/O PRODUCTS, INC.

10623 Roselle Street, San Diego, CA 9212 • (858) 550-9559 • Fax (858) 550-7322
contactus@accesio.com • www.accesio.com

MODEL 104-AI12-AIM

USER MANUAL

FILE: 104-AI12-AIM.A1g

Notice

The information in this document is provided for reference only. ACCES does not assume any liability arising out of the application or use of the information or products described herein. This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of ACCES, nor the rights of others.

IBM PC, PC/XT, and PC/AT are registered trademarks of the International Business Machines Corporation.

WARNING!!

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A BOARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING BOARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O BOARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

Warranty

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

Terms and Conditions

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

Coverage

First Three Years: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

Equipment Not Manufactured by ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

General

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

Table of Contents

Chapter 1: Introduction

This is a PC/104, eight channel, 12 bit resolution analog input board. Based on the Maxim 197 Analog to Digital Converter (A/DC), this circuit provides good specs at a very low cost per channel. It is intended to be used together with a PC/104 analog input multiplexer board to provide a complete solution for sensor to computer interface applications. This board may receive analog signals from up to seven such sub-multiplexer boards. The user's software may select a channel for conversion, specify a voltage range, and choose either bipolar or unipolar mode with a single command. The A/DC end-of-conversion may generate an interrupt or the user's software may poll the busy-bit to determine when data is valid. Refer to the Programming and Calibration chapters for further information.

Technical Specification

Analog Inputs

- Channels/type: 8 single-ended
- Conversion Frequency: 100K samples per second
- Resolution: 12-bit
- Gain Temperature Coefficient: 5ppm/°C typical, bipolar
  3ppm/°C typical, unipolar
- Gain Error: ±10 LSB
- Integral Nonlinearity: ±1 LSB maximum
- Differential Nonlinearity: ±1 LSB
- Unipolar Offset Error: ±5 LSB
- Bipolar Offset Error: ±10 LSB
- Accuracy: 0.2% of full scale
- Noise Levels: ±1 LSB typical
- Programmable Voltage Ranges: 0-5V, 0-10V, ±5V, ±10V

General

- Power Required: +5V @ 50mA
- Interrupt Requests: Eleven channels, IRQ 3-7, 9-12, 14, 15
- Environmental: -40°C to +85°C

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing serial ports under linux.

Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

To Install the Board

1. Install jumpers for selected options and base address according to your application requirements, as mentioned above.
2. Remove power from the PC/104 stack.
3. Assemble standoff hardware for stacking and securing the boards.
4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
6. Check that all connections in your PC/104 stack are correct and secure then power up the system.
7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

Chapter 3: Option Selection

The board's base address and IRQ channel are the only jumper selectable options. Voltage input ranges are selected via software. Special signal conditioning for different input types are factory installed options.

Jumpers are available on the board to configure the following options:

1. Base address
2. IRQ level

You may also refer to the Setup Program Utility on the provided CD for details of selecting the appropriate options for your application.

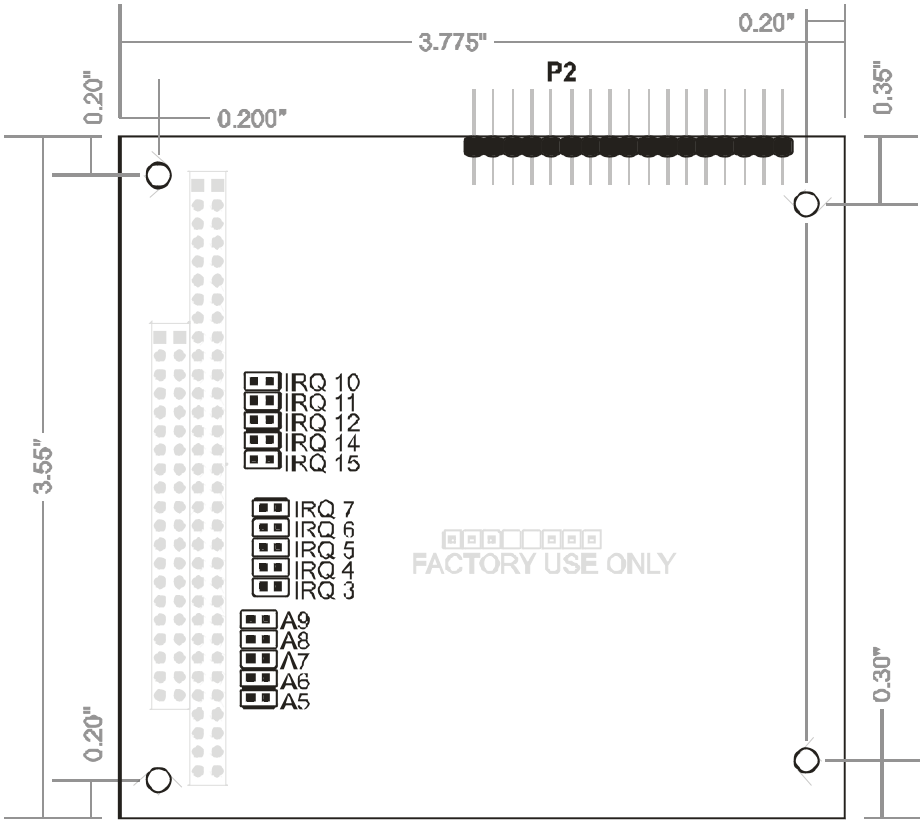


Figure 3-1: A/D Option Selection Map

Chapter 4: Address Selection

The board base address on the I/O bus is set by JUMPERS next to the PC/104 connector. The jumper posts are marked A5 through A9 and A5 is the least significant bit of the address. The base addresses can be selected anywhere within the I/O address range 100-3FF provided that they do not overlap with other functions. The FINDBASE software utility provided on CD with your board will help you select a base address that does not conflict with other assignments. If in doubt, refer to the following table for a list of standard address assignments.

In order to configure the desired address, the hexadecimal address must be converted to a binary representation.

For example, as illustrated below, jumper selection corresponds to hex **2C0 (or binary 10 101xxxxx).** The "xxxxx" represents address lines A4 through A0 used on the board to select individual registers as described in the Chapter 5, Programming of the manual.

Hex Representation	2		C		
Conversion Factors	2	1	8	4	2
Binary Representation	1	0	1	1	0
Jumper Setting	Out	In	Out	Out	In
Jumper Label	A9	A8	A7	A6	A5

Table 4-1: Hex Representation

Please note that “1" = “out”(no jumper) and “0" = “in”(jumper installed).

Review the Address Selection Table carefully before selecting the board address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. If you have doubts concerning available addresses in your particular computer, use the FINDBASE utility provided to determine available addresses.

The following table provides a convenient reference for all address jumper configurations. ON indicates the jumper is installed.

A9	A8	A7	A6	A5	Address Range
					3E0h - 3FFh
				ON	3C0h - 3DFh
			ON		3A0h - 3BFh
			ON	ON	380h - 39Fh
		ON			360h - 37Fh
		ON		ON	340h - 35Fh
		ON	ON		320h - 33Fh
		ON	ON	ON	300h - 31Fh
	ON				2E0h - 2FFh
	ON			ON	2C0h - 2DFh
	ON		ON		2A0h - 2BFh
	ON		ON	ON	280h - 29Fh
	ON	ON			260h - 27Fh
	ON	ON		ON	240h - 25Fh
	ON	ON	ON		220h - 23Fh
	ON	ON	ON	ON	200h - 21Fh
ON					1E0h - 1FFh
ON				ON	1C0h - 1DFh
ON			ON		1A0h - 1BF
ON			ON	ON	180h - 19Fh
ON		ON			160h - 17Fh
ON		ON		ON	140h - 15Fh
ON		ON	ON		120h - 13Fh
ON		ON	ON	ON	100h - 11Fh

Table 4-2: Converting Base Addresses To Jumper Settings

Chapter 5: Programming

The board uses 4 consecutive registers in I/O space as follows:

Offset	Read Function	Write Function
00h	Board Status / Clear Board Status	IRQ Clear
01h	Interrupt Status	Interrupt Enables
02h	A/DC Low Byte	Start A/D Conversion
03h	A/DC High Byte	

Base + 0: **Board Status**

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
READ	A/DC EOC	reserved	reserved	reserved	reserved	IRQ Enabled	reserved	reserved

This register shows the state of the two events that can generate interrupts (IRQs), and the state of the global interrupt enable. The interrupt enables/disables have no affect on the events shown in this register. All bits are active HIGH. Also, all of the event bits are latched; when an event occurs, its bit goes HIGH until this register is read. Reading this register clears it.

Writing to this register clears IRQs (see the description of IRQ enables).

Bit 7 goes HIGH when an A/D conversion completes (used for simple A/D acquisition).

Bit 2 reflects the global interrupt enable written to Base + 1. This is not an event, and is not cleared when read.

Base + 1: **Interrupt Enables, Interrupt Status**

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
READ	A/DC IRQ	reserved	reserved	reserved	reserved	IRQ Event	always zero	always zero
WRITE	A/DC IRQ Enable	reserved	reserved	reserved	reserved	Global IRQ Enable	reserved	reserved

All bits are active HIGH. Reading this address accesses the Status register. Writing to this address affects the Enables register. Note that the register that's written to is not the same register that's read at this address.

Interrupts from this board can be shared. The IRQ driver will pull the PC/104 interrupt line LOW for 500nS, briefly drive it HIGH, and then tri-state. After an interrupt is generated another won't be allowed until the IRQ has been cleared (write to Base+0) and the data read (for some event types).

Set bit 2 HIGH to enable interrupts from the board. The default after system RESET is LOW. Without this global enable set, the board will not generate interrupts of any kind. If an interrupt has been generated by the board, this bit will be HIGH when read.

Set bit 7 HIGH to enable interrupts from the A/DC. When read, bit 7 is HIGH if the A/DC generated an interrupt that was not yet cleared. Read Base+2 and Base+3 to get the A/D data, and write to Base+0 to clear the board's interrupt so it can generate another.

USING THE ANALOG TO DIGITAL CONVERTER

This circuit is based on a Maxim ADC chip. Please refer to file MAX197.pdf in the \CHIPDOCS directory on the CDROM. A conversion begins when a control byte is written to the ADC. The control byte contains five bit fields: channel selection, bipolar/unipolar, range, acquisition mode, and device mode. Normally, the acquisition mode and device mode bits will be zero.

Base + 2: **A/D Control Byte**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Mode 1	Device Mode 0	Acquisition Mode	Range	Bipolar / Unipolar	Channel Selection Bit 2	Channel Selection Bit 1	Channel Selection Bit 0

The two bits in the device mode field select the clock source and the power state. Before putting the ADC in a power down state, a conversion with Normal Operation selected should be triggered. The chip will 'remember' this clock setting if the Standby power-down mode is subsequently used. The Standby state is entered after a conversion is complete, there is no start-up delay on the next conversion. There is a 50mS start-up delay before a conversion from the full power-down state.

Bit 7	Bit 6	Device Mode
0	0	Normal Operation, selects the external (to the ADC) clock mode, a 2MHz clock frequency is applied
0	1	Internal clock mode, not appropriate for this circuit, unexpected events may occur if this mode is selected
1	0	Standby power-down, supply current will typically be 700uA
1	1	Full power-down, supply current will be 120uA worst case

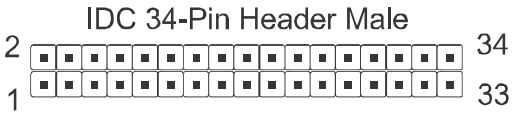
The ADC has a Sample and Hold circuit controlled by the Acquisition Mode bit. A control byte with this bit set low will select an acquisition interval of 3uS after which a conversion will begin. A noisy signal may require more integration. A control byte with this bit set high will start a user-determined acquisition period, conversion will begin when a 2nd control byte is sent with bit 5 set low.

Range (Bit 4)	Bipolar / Unipolar (Bit 3)	Input Range
0	0	0 - 5V
1	0	0 - 10V
0	1	±5V
1	1	±10V

Bits 0, 1, and 2 must be the same value but the power state may be changed.
Bit 4, the range bit, doubles the input voltage range when set.
Bit 3 selects bipolar mode when set.
The channel selection bits direct one of the eight analog inputs connected to the ADC's multiplexer to the Sample and Hold circuit. Bits 2, 1, and 0 make a binary value equal to the channel number.

A/D data is at Base +2 and +3, usually read as a single 16-bit read. In bipolar modes it is in two's complement format.

Chapter 6: Connector Pin Assignments



A/D Board P2				
Pin #	**Signal**		**Pin #**	**Signal**
1	A/D Reference Voltage Output		18	
2	Reference Adjust Input		19	GROUND
3	GROUND		20	
4			21	
5			22	Channel 4 Input
6	Channel 0 Input		23	GROUND
7	GROUND		24	Channel 5 Input
8	Channel 1 Input		25	
9			26	
10			27	GROUND
11	GROUND		28	
12			29	
13			30	Channel 6 Input
14	Channel 2 Input		31	GROUND
15	GROUND		32	Channel 7 Input
16	Channel 3 Input		33	
17			34	

Appendix A: Connecting A/D to Submultiplexer

The A/D board is one part of a four piece kit (PC/104 32-Channel Analog Input Signal Conditioner, PC/104 A/D board, interconnecting ribbon cable and one set of PC/104 metric mounting hardware. It may be connected from the analog input multiplexer (mux) with the provided one inch ribbon cable at P3 (the submultiplexer output) to P2 (the A/DC input). Each submultiplexer board's output connects to one of eight inputs on the A/D board. Seven mux cards and one A/DC card comprise a full system. Note that the eighth A/DC input is commonly connected to a temperature sensor placed on the mux cards (see the submultiplexer board's manual).

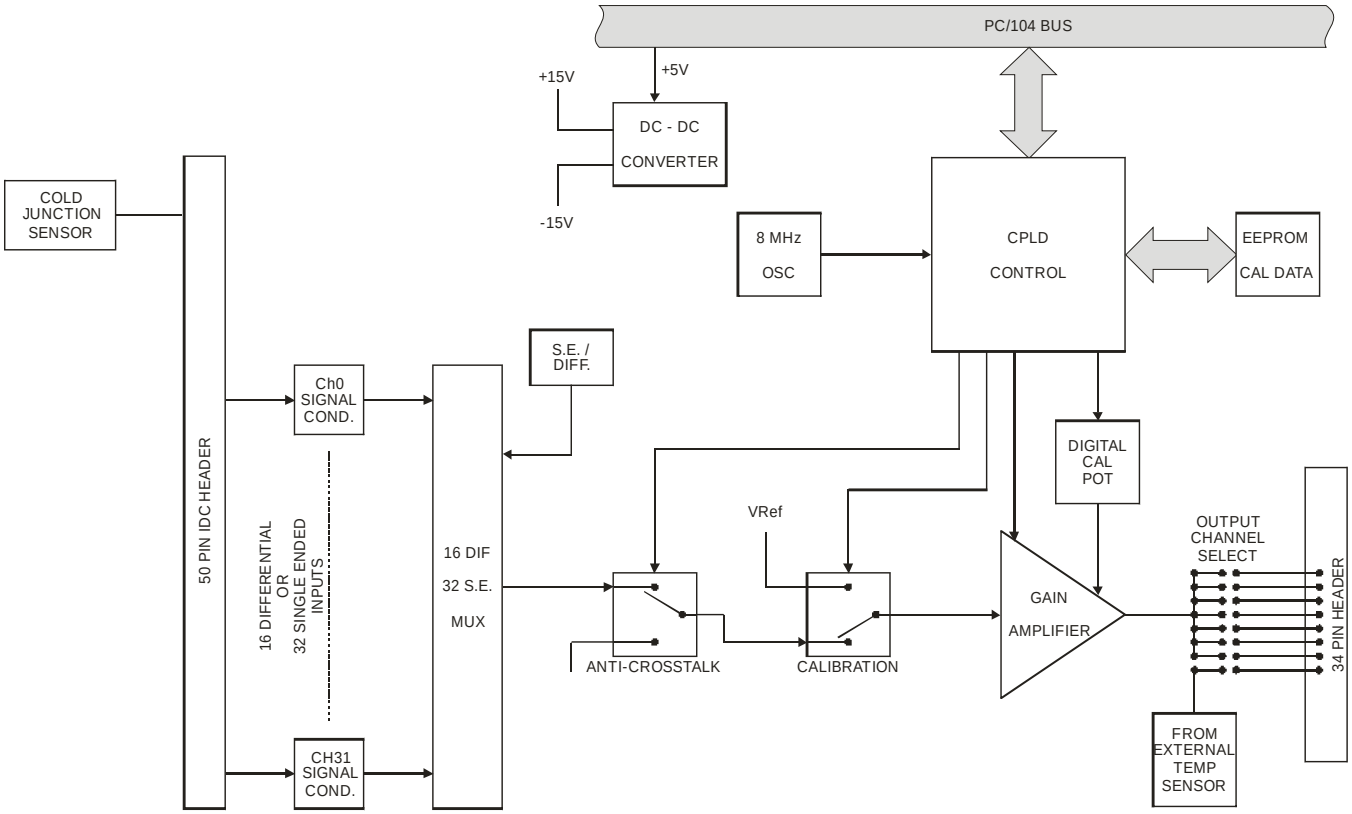


Figure A-1: Submultiplexer Block Diagram

104-AI12-AIM

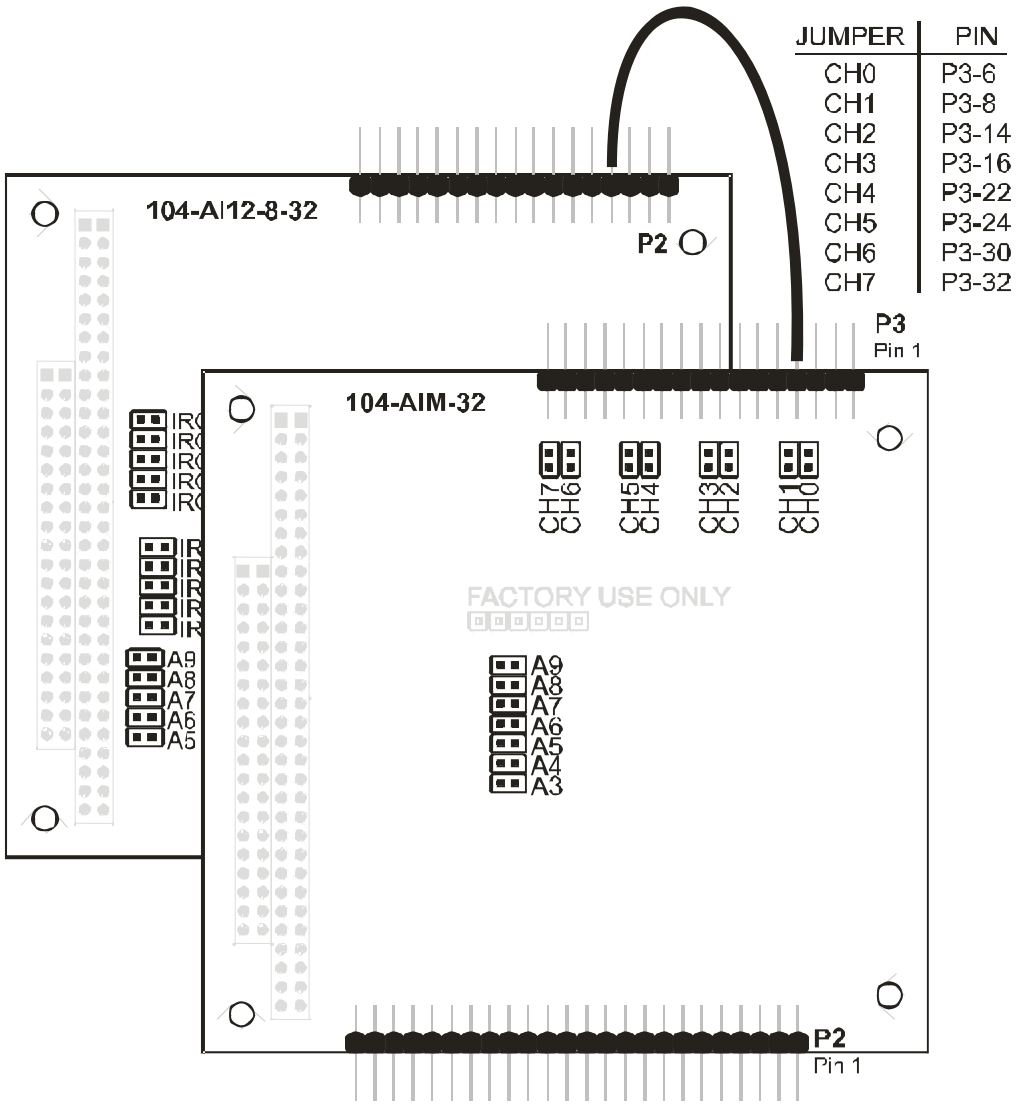


Figure A-2: Connection Diagram

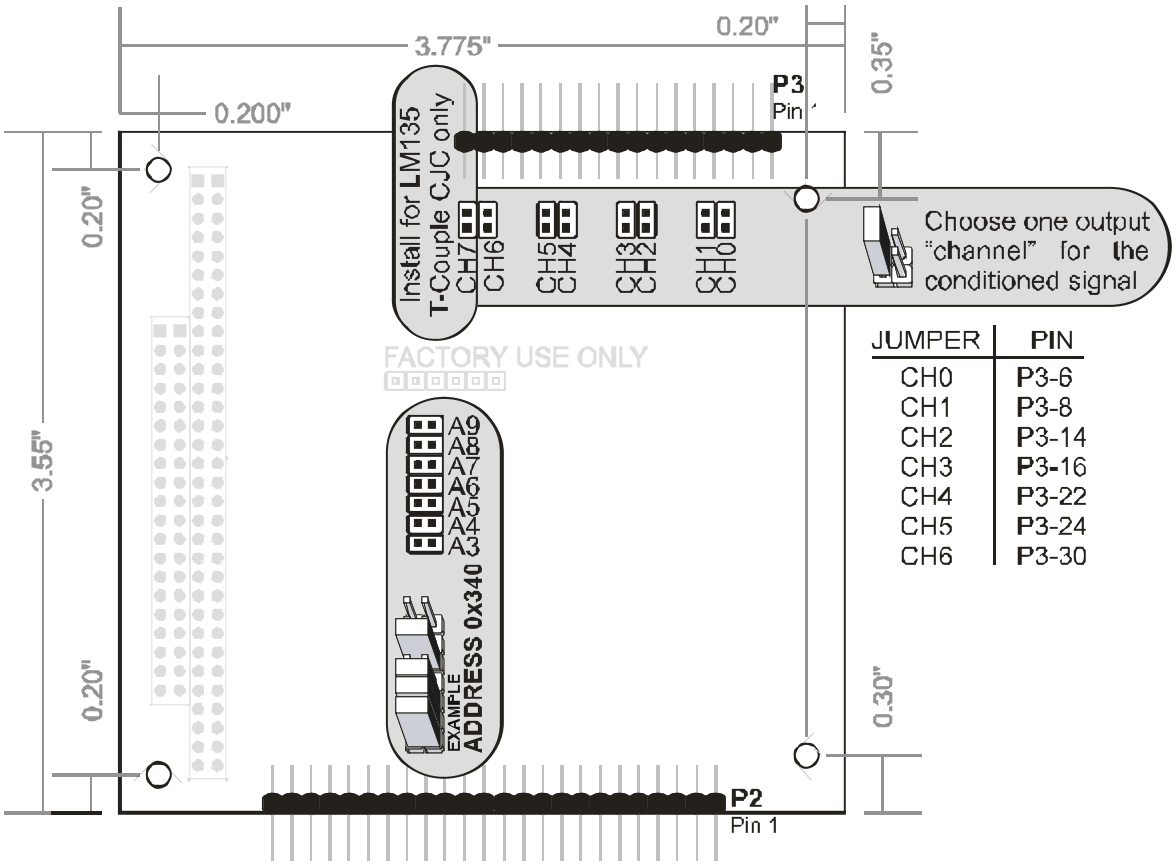


Figure A-3: Submultiplexer Option Selection Map

This figure is an excerpt from the submultiplexer's user manual. The kit includes a cable that would be connected to P3 on this drawing. A jumper would be placed on one set of the jumper pins labeled CH0 through CH6. If the submultiplexer has a temperature sensor installed a jumper would be placed on the CH7 pins.

Channel 7 of the A/D board often connects to an ambient temperature sensor mounted on the (optional) input 50-pin screw terminal adapter board of the submultiplexer and must not have any active circuit between the P2 connector and the A/DC chip. This is also true for any multiplexer board's output.

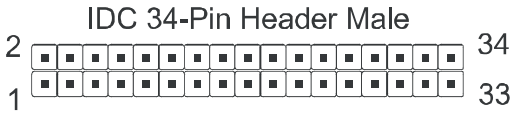


Table A-1: Submultiplexer Connector P3

Pin #	Signal Name	Pin #	Signal Name
1	Voltage Reference	18	no connection
2	no connection	19	GROUND
3	GROUND	20	no connection
4	no connection	21	no connection
5	no connection	22	CHANNEL 4
6	CHANNEL 0	23	GROUND
7	GROUND	24	CHANNEL 5
8	CHANNEL 1	25	no connection
9	no connection	26	no connection
10	no connection	27	GROUND
11	GROUND	28	no connection
12	no connection	29	no connection
13	no connection	30	CHANNEL 6
14	CHANNEL 2	31	GROUND
15	GROUND	32	CHANNEL 7
16	CHANNEL 3	33	GROUND
17	no connection	34	no connection

This table is an excerpt from the submultiplexer's user manual. The signal names correspond to the output channel jumpers. This table is useful if the cable supplied with the kit is not used.

Table A-2: Submultiplexer Connector P2, **Single-Ended Inputs**

Pin #	Signal Name	Pin #	Signal Name
1	CH00	26	GROUND
2	CH16	27	CH08
3	GROUND	28	CH24
4	CH01	29	GROUND
5	CH17	30	CH09
6	GROUND	31	CH25
7	CH02	32	GROUND
8	CH18	33	CH10
9	GROUND	34	CH26
10	CH03	35	GROUND
11	CH19	36	CH11
12	GROUND	37	CH27
13	CH04	38	GROUND
14	CH20	39	CH12
15	GROUND	40	CH28
16	CH05	41	GROUND
17	CH21	42	CH13
18	GROUND	43	CH29
19	CH06	44	GROUND
20	CH22	45	CH14
21	GROUND	46	CH30
22	CH07	47	GROUND
23	CH23	48	CH15
24	GROUND	49	CH31
25	TEMPERATURE SENSOR	50	GROUND

This table is an edited excerpt from the submultiplexer's user manual. Any single input can be selected by the multiplexer via software commands to be applied to the amplifier circuit. A five bit field in the command byte selects which input to amplify or attenuate and present to the A/DC. For example, xxx10000b would select the signal on pin 2.

Table A-3: Submultiplexer Connector P2, **Differential Inputs**

Pin #	Signal Name	Pin #	Signal Name
1	CH00+	26	GROUND
2	CH00 -	27	CH08+
3	GROUND	28	CH08 -
4	CH01+	29	GROUND
5	CH01 -	30	CH09+
6	GROUND	31	CH09 -
7	CH02+	32	GROUND
8	CH02 -	33	CH10+
9	GROUND	34	CH10 -
10	CH03+	35	GROUND
11	CH03 -	36	CH11+
12	GROUND	37	CH11 -
13	CH04+	38	GROUND
14	CH04 -	39	CH12+
15	GROUND	40	CH12 -
16	CH05+	41	GROUND
17	CH05 -	42	CH13+
18	GROUND	43	CH13 -
19	CH06+	44	GROUND
20	CH06 -	45	CH14+
21	GROUND	46	CH14 -
22	CH07+	47	GROUND
23	CH07 -	48	CH15+
24	GROUND	49	CH15 -
25	TEMPERATURE SENSOR	50	GROUND

This table is an edited excerpt from the submultiplexer's user manual. Differential pairs are selected with software commands and connected to the signal conditioning circuit. For example, xxxx0001 would select the signals on pins 4 and 5.

System Calibration

A multi-meter that can measure voltage as low as 780uV is required to accurately calibrate the submultiplexer. Also, a voltage calibrator or a stable, noise-free, DC voltage source that can be used in conjunction with the digital multi-meter is required for best results.

The submultiplexer's signal-conditioning circuit (that part which amplifies, attenuates, or level-shifts) may be calibrated independently. Six bytes (one per voltage range) for offsets and six bytes for gain adjustments are stored in the board's EEPROM for each input (16 diff. or 32 S.E.). Software is provided that will totally automate this internal calibration. Run the calibration program and follow the prompts.

The board comes with a calibration program that, in conjunction with current or voltage sources and meters and user interaction, will calibrate the system. Voltage offsets at the board's input pins plus any offset generated on the board plus offset from the A/DC can be nulled out. Gain adjustment of +5% can be saved in the EEPROM for each input (up to 32 signals) times each voltage range.

The submultiplexer accepts a mix of differential and single-ended inputs. There is a specific location in the board's EEPROM for each signal's offset adjustment and gain adjustment. For example, assume that a differential signal is connected to P2 pins 1 and 2. The DC offset and gain adjust values should be written to the board's EEPROM at 0h and 100h for the +10V range, at 20h and 120h for the +5V range, etc. Refer to the EEPROM memory map to identify the locations required.

1. If possible, set the output of a signal to be measured to 0V.
2. Write 0h to the Setup register if the signal channel to be calibrated is differential. Write 11h for single-ended signals.

Bit 7, Bit 6, Bit 5	Voltage Range	Gain
0 0 0	+10	0.5
0 0 1	+5	1.0
0 1 0	+2.5	2.0
0 1 1	+100mV	50
1 0 0	+50mV	100
1 0 1	+25mV	200

Table A-4: Range Selection

3. Write 80h to the EEPROM at the offset adjust and gain adjust addresses for the signal channel to be calibrated. The EEPROM requires approximately 1mS to store a byte, a 'busy' bit is set in the Setup byte while this happens.
4. The Command register has two fields: the channel number (bits 0 through 4) and the range selection. For the signal channel to be calibrated, write the combined range and channel to the Command register. The board will retrieve data from the EEPROM and load it in the digital pots each time a byte is written to the Command register.
5. Use the A/DC connected to the output of the submultiplexer to digitize the voltage. Adjust the value of the calibration value to compensate for any DC offset.
6. If possible, set the voltage of the signal to a value near the top of its range. Trigger a conversion and adjust the value in the EEPROM up or down until the output of the system is correct.
7. Repeat these steps for all of the channels in use.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

10623 Roselle Street, San Diego CA 92121-1506
Tel. (858) 550-9559 FAX (858) 550-7322
www.accesio.com