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MODEL IOD-48S

USER MANUAL

FILE: iod-48s

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- 48 Bits of Digital Input/Output.
- Interrupt Generation on Input Change of State.
- Change-of-state Interrupt Software Enabled in Six 8-Input Ports.
- All 48 I/O Lines Buffered on the Board.
- I/O Buffers Can Be Enabled/Disabled under Program Control.
- Four and Eight Bit Ports Independently Selectable for I/O.
- Pull-Ups on I/O Lines.
- +5V Supply Available to the User.
- Compatible with Industry Standard I/O Racks like Gordos, Opto-22, Potter & Brumfield, etc.

Applications

- Automatic Test Systems.
- Laboratory Automation.
- Robotics.
- Machine Control.
- Security Systems, Energy Management.
- Relay Monitoring and Control.
- Parallel Data Transfer to PC.
- Sensing Switch Closures or TTL, DTL, CMOS Logic.
- Driving Indicator Lights or Recorders.

Description

The state of all inputs can be monitored and, if any one or more bits change state, a latched interrupt request can be generated. Thus, it is not necessary to use software to continuously poll the inputs to detect a change of state. The change-of-state interrupt is enabled by a software write to an interrupt-enable register. Six bits in that register each control an eight-input port at one of two type 8255-5 Programmable Peripheral Interface chips. The change-of-state interrupt latch can be cleared by a software write.

Also, bit C3 at each 24-bit port can be used as an external interrupt to the computer if jumpers are installed. When bit C3 goes high (edge triggering), an interrupt is requested. Interrupts from the ports are OR'ed together and OR'ed with the change-of-state interrupt. Interrupts are directed to levels #2 through #7, #10 through #12, #14 and #15 by jumper installation.

The IOD-48S card was designed for industrial applications and can be installed in 16-bit ISA bus slots of IBM PC/XT/AT or compatible computers. Each I/O line is buffered and capable of sourcing 15 mA or sinking 24mA (64 mA on request). The card contains two Programmable Peripheral Interface chips type 8255-5 (PPI) to provide computer interface to 48 I/O lines. Three 8-bit ports A, B, and C. Each 8-bit port can be software configured to function as either inputs or output latches. Port C can also be configured as four inputs and four output latches. Pull-ups on the card assure that there are no erroneous outputs at power up until the card is initialized by system software.

Tristate I/O line buffers (74LS245) are configured automatically by hardware logic for input or output use according to direction assignment from a control register in the PPI. Further, if a jumper is properly placed on the card, the tristate buffers are enabled/disabled under program control. (See the Option Selection section to follow.)

I/O wiring connections are via 50-pin headers on the board. Two flat I/O cables connect IOD-48S to termination. Also, this provides compatibility with OPTO-22, Gordos, Potter & Brumfield, and all module mounting racks. Every second conductor of the flat cables is grounded to minimize the effect of crosstalk between signals. If needed for external circuits, +5 VDC power is available on each I/O connector pin 49. If you use this power, we recommend that you include a 1A fast-blow fuse in your circuits in order to avoid possible damage to the host computer or cable in the event of a malfunction in those external circuits.

The IOD-48S occupies sixteen bytes of I/O address space. The base address is selectable via a DIP switch anywhere within the range of 000-3F0 hex. An illustrated setup program is provided with the IOD-48S card. Interactive displays show locations and proper settings of DIP switches and jumpers to set up board address, interrupt levels, and interrupt enable. Also, sample programs in Turbo-C and Turbo-Pascal are presented in the Software section of this manual.

Specification

Digital Inputs (TTL Compatible)

- Logic High: 2.0 to 5.0 VDC.
- Logic Low: -0.5 to +0.8 VDC.
- Input Load (Hi): 20 uA.
- Input Load (Lo): -200 uA.

Digital Outputs

- Logic High: 2.5 VDC min., source 15 mA.
- Logic Low: 0.5 VDC max., sink 24 mA.
  (64 mA optional)

- Power Output: +5 VDC from computer bus (ext. 1A fast-blow fuse recommended).
- Power Required: +5 VDC at 300 mA typical.
- Size: 7.15" Long (182 mm)

Environmental

- Operating Temperature: 0 °C. to 60 °C.
- Storage Temperature: -50 °C. to +120 °C.
- Humidity: 0 to 90% RH, non-condensing.

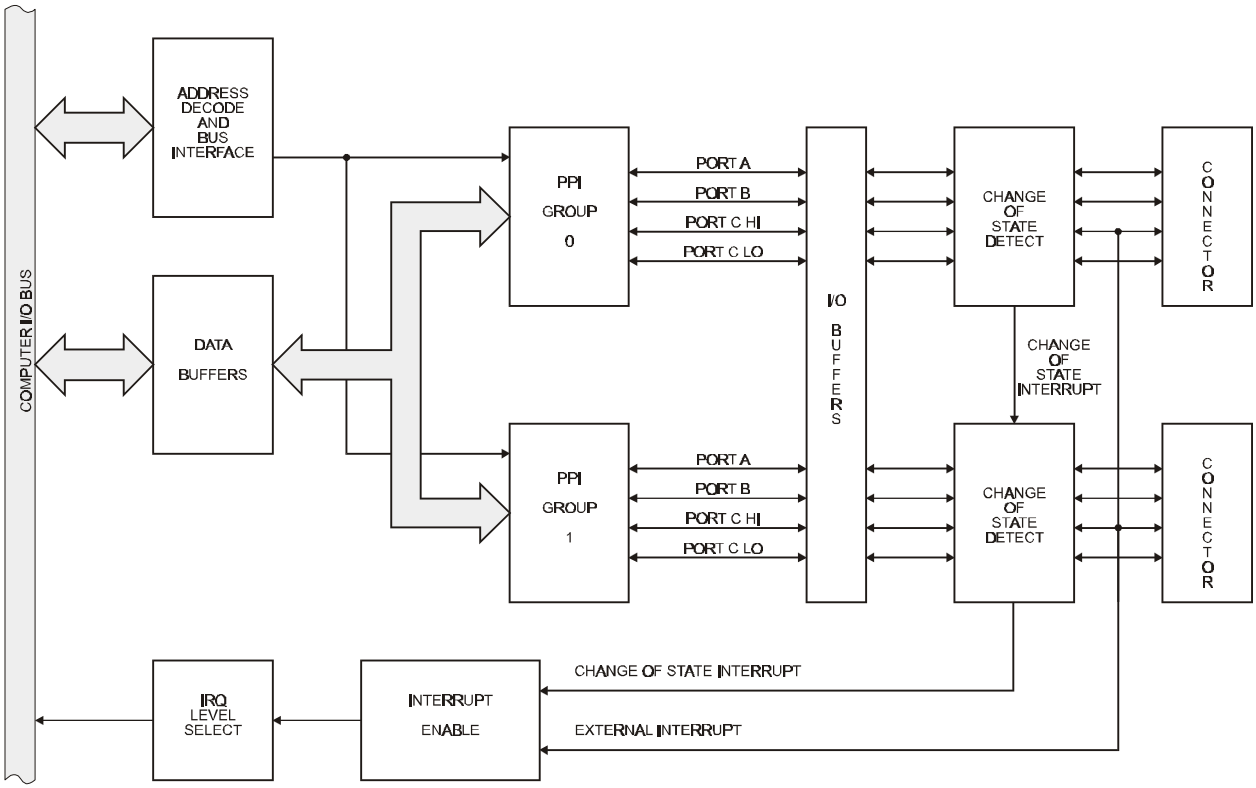


Figure 1-1: IOD-48S Block Diagram

Chapter 2: Installation

The software provided with this card is contained on either one CD or multiple diskettes and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your software format and operating system. Substitute the appropriate drive letter for your CD-ROM or disk drive where you see d: or a: respectively in the examples below.

CD Installation

DOS/WIN3.x

1. Place the CD into your CD-ROM drive.
2. Type d:K to change the active drive to the CD-ROM drive.
3. Type installK to run the install program.
4. Follow the on-screen prompts to install the software for this card.

WIN95/98/NT

1. Place the CD into your CD-ROM drive.
2. The CD should automatically run the install program after 30 seconds. If the install program does not run, click START | RUN and type d:install, click OK or press K.
3. Follow the on-screen prompts to install the software for this card.

3.5-Inch Diskette Installation

As with any software package, you should make backup copies for everyday use and store your original master diskettes in a safe location. The easiest way to make a backup copy is to use the DOS DISKCOPY utility.

In a single-drive system, the command is:

diskcopy a: a:K

You will need to swap disks as requested by the system.
In a two-disk system, the command is:

diskcopy a: b:K

This will copy the contents of the master disk in drive A to the backup disk in drive B.

To copy the files on the master diskette to your hard disk, perform the following steps.

1. Place the master diskette into a floppy drive.
2. Change the active drive to the drive that has the diskette installed. For example, if the diskette is in drive A, type a:K.
3. Type installK and follow the on-screen prompts.

Directories Created on the Hard Disk

The installation process will create several directories on your hard disk. If you accept the installation defaults, the following structure will exist.

[CARDNAME]

Root or base directory containing the SETUP.EXE setup program used to help you configure jumpers and calibrate the card.

DOS\PSAMPLES: A subdirectory of [CARDNAME] that contains Pascal samples.
DOS\CSAMPLES: A subdirectory of [CARDNAME] that contains "C" samples.
Win32\language: Subdirectories containing samples for Win95/98 and NT.

WinRisc.exe

A Windows dumb-terminal type communication program designed for RS422/485 operation. Used primarily with Remote Data Acquisition Pods and our RS422/485 serial communication product line. Can be used to say hello to an installed modem.

ACCES32

This directory contains the Windows 95/98/NT driver used to provide access to the hardware registers when writing 32-bit Windows software. Several samples are provided in a variety of languages to demonstrate how to use this driver. The DLL provides four functions (InPortB, OutPortB, InPort, and OutPort) to access the hardware.

This directory also contains the device driver for Windows NT, ACCESNT.SYS. This device driver provides register-level hardware access in Windows NT. Two methods of using the driver are available, through ACCES32.DLL (recommended) and through the DeviceIOControl handles provided by ACCESNT.SYS (slightly faster).

SAMPLES

Samples for using ACCES32.DLL are provided in this directory. Using this DLL not only makes the hardware programming easier (MUCH easier), but also one source file can be used for both Windows 95/98 and WindowsNT. One executable can run under both operating systems and still have full access to the hardware registers. The DLL is used exactly like any other DLL, so it is compatible with any language capable of using 32-bit DLLs. Consult the manuals provided with your language's compiler for information on using DLLs in your specific environment.

VBACCES

This directory contains sixteen-bit DLL drivers for use with VisualBASIC 3.0 and Windows 3.1 only. These drivers provide four functions, similar to the ACCES32.DLL. However, this DLL is only compatible with 16-bit executables. Migration from 16-bit to 32-bit is simplified because of the similarity between VBACCES and ACCES32.

PCI

This directory contains PCI-bus specific programs and information. If you are not using a PCI card, this directory will not be installed.

SOURCE

A utility program is provided with source code you can use to determine allocated resources at run-time from your own programs in DOS.

PCIFind.exe

A utility for DOS and Windows to determine what base addresses and IRQs are allocated to installed PCI cards. This program runs two versions, depending on the operating system. Windows 95/98/NT displays a GUI interface, and modifies the registry. When run from DOS or Windows3.x, a text interface is used. For information about the format of the registry key, consult the card-specific samples provided with the hardware. In Windows NT, NTioPCI.SYS runs each time the computer is booted, thereby refreshing the registry as PCI hardware is added or removed. In Windows 95/98/NT PCIFind.EXE places itself in the boot-sequence of the OS to refresh the registry on each power-up.

This program also provides some COM configuration when used with PCI COM ports. Specifically, it will configure compatible COM cards for IRQ sharing and multiple port issues.

WIN32IRQ

This directory provides a generic interface for IRQ handling in Windows 95/98/NT. Source code is provided for the driver, greatly simplifying the creation of custom drivers for specific needs. Samples are provided to demonstrate the use of the generic driver. Note that the use of IRQs in near-real-time data acquisition programs requires multi-threaded application programming techniques and must be considered an intermediate to advanced programming topic. Delphi, C++ Builder, and Visual C++ samples are provided.

Findbase.exe

DOS utility to determine an available base address for ISA bus , non-Plug-n-Play cards. Run this program once, before the hardware is installed in the computer, to determine an available address to give the card. Once the address has been determined, run the setup program provided with the hardware to see instructions on setting the address switch and various option selections.

Poly.exe

A generic utility to convert a table of data into an nth order polynomial. Useful for calculating linearization polynomial coefficients for thermocouples and other non-linear sensors.

Risc.bat

A batch file demonstrating the command line parameters of RISCTerm.exe.

RISCTerm.exe

A dumb-terminal type communication program designed for RS422/485 operation. Used primarily with Remote Data Acquisition Pods and our RS422/485 serial communication product line. Can be used to say hello to an installed modem. RISCTerm stands for Really Incredibly Simple Communications TERMinal.

Installing the Card

Before installing the card carefully read the Address Selection and Option Selection Sections of this manual and configure the card according to your requirements. Use the special software program called SETUP provided on CD with the card. It supplies visual aids to configure all areas of the board.

Be especially careful with address selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. If unsure what locations are available, you can use the FINDBASE program provided on our CD to locate blocks of available addresses.

To Install the Card

1. Remove power from the computer.
2. Remove the computer cover.
3. Remove blank I/O backplate.
4. Install jumpers for selected options. See Option Selection
5. Select the base address on the card. See Address Selection
6. Loosen the nuts on the strain relief bar and swing top end free.
7. Install the card in an I/O expansion slot. If convenient, select a slot adjacent to a vacant slot because this will make cable installation easier.
8. Thread the I/O cables, one by one, through the cutout in the mounting bracket and plug them into the headers.
9. Smooth the cables as close as possible to the card and, while holding them close to the surface of the card, swing the strain relief bar into position and tighten nuts.
10. Inspect for proper fit of the card and cables and tighten screws.
11. Replace the computer cover.

Input/Output connections are via two 50-pin headers on the card. A blank mounting bracket is provided with units that are marked for CE (European) Certification and for these units CE-certifiable cable and break-out methodology (cables connect to chassis ground at the aperture, shielded twisted pair wiring, etc.) must be used. Also, it is important that the card mounting bracket be properly screwed into place and that there be a positive chassis ground.

Chapter 3: Option Selection

Refer to the setup programs provided with the card. Also, refer to the Block Diagram on Page 1-4 and the Option Selection Map on the following page when reading this section of the manual.

External Interrupts are accepted on the I/O connector pin 9 (bit C3). The Interrupt signal is positive true. External Interrupts are enabled if the IEN jumper is installed. Interrupts are directed to levels #2 through #7, #10 through #12, #14 and #15 by jumpers installed at locations labeled IRQ2 through IRQ7, IRQ10 through IRQ12, IRQ14 and IRQ15 respectively.

A means of enabling or disabling the 74LS245 input/output buffers under program control is provided at the jumper position labeled TST/BEN. When the jumper is in the BEN (Buffer Enable) position, the I/O buffers are always enabled. When the jumper is in the TST (Tristate) position, enabled/disabled state is controlled by a control register. (See the programming section of this manual for a description.)

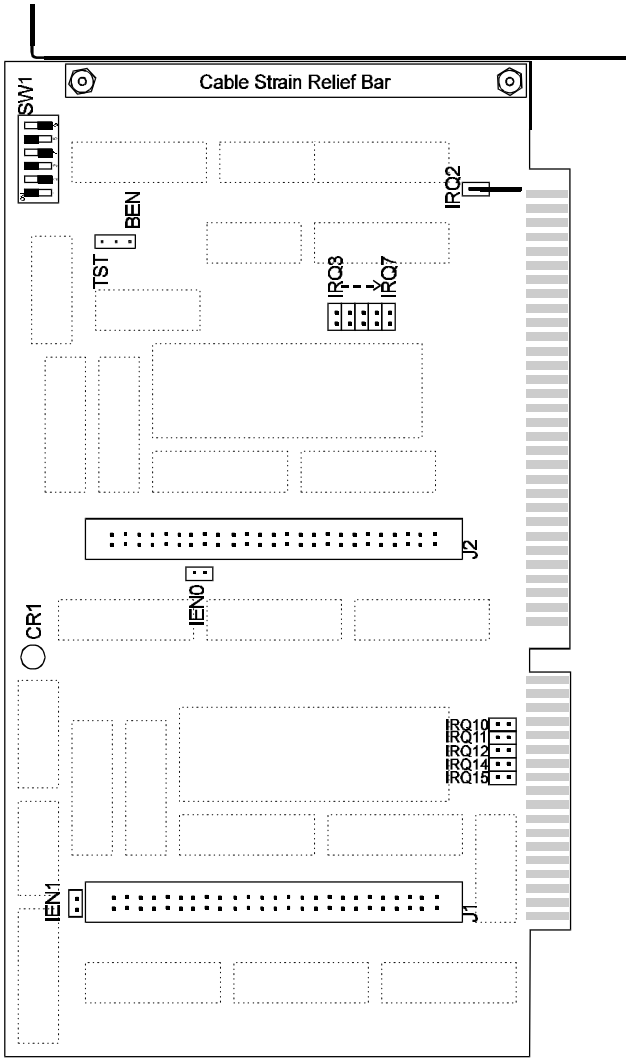
An LED, CR1, is provided at the top-center of the card to assist you in program development. Each time an interrupt is generated, the LED will illuminate and remain on until the interrupt is reset. If there is an immediate reset of the interrupt, it is likely that the LED will not remain on long enough to be observed.

Note

A jumper must be installed in either the TST or the BEN position for the card to function.

There is a wire jumper installed on the card at a position labeled WAIT. The associated circuitry asserts a WAIT signal to the CPU in order to provide a longer write cycle. In this way, there is assurance that the 8255 PPI. will have adequate time to accept inputs from the CPU in fast AT computers. If this extra wait state will cause a problem in your application and if you deem it non-essential, then this wire jumper may be clipped.

The foregoing are the only manual setups necessary to use the IOD-48S. Input/Output selection and the change-of-state Interrupt Enable is done via software by writing to a control register in each PPI as described in the Programming section of this manual.



Switch:
SW1=Base Address

Jumpers:
TST/BEN=Buffer DIsable/Buffer Enable Jumper
IEN0=External Interrupt Enable on PPI #0
IEN1=External Interrupt Enable on PPI #1
IRQ2-IRQ7, IRQ10-12, IRQ14-15=Select IRQ level

LEDs:
CR1=Interrupt Indication LED.

Figure 3-1: IOD-48S Option Selection Map

Chapter 4: Address Selection

The IOD-48S card occupies 16 bytes of I/O space. The card base address can be selected anywhere within the I/O address range 100-3F0 hex in AT's (except 1F0 to 1F8) and 200-3F0 in XT's. If in doubt where to assign the base address, refer to the following tables and the FINDBASE program to find an available address for your system.

Hex Range	Usage
000-01F	DMA Controller 1
020-03F	INT Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real Time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	INT Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Coprocessor
0F8-0FF	Arithmetic Processor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Asynchronous Comm'n (Secondary)
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC or Binary Synchronous Comm'n 2
3A0-3AF	Binary Synchronous Comm'n 1
3B0-3BF	Monochrome Display/Printer
3C0-3CE	Local Area Network
3D0-3DF	Color/Graphic Monitor
3F0-3F7	Floppy Diskette Controller
3F8-3FF	Asynchronous Comm'n (Primary)

Table 4-1: Standard Address Assignments for 286/386/486 Computers

To set desired board address , refer to the illustrated Board Address setup program on the CD provided with the card. Type the desired address in hexadecimal code and the graphic display shows you how to set the Address Setup switches. These switches are marked A4-A9 and form a binary representation of the address in negative-true logic. (assign '0' to all Address Setup switches turned ON, and assign '1' to all Address Setup switches turned OFF.)

Switch Identification	A9	A8	A7	A6	A5	A4
Address Line Controlled	A9	A8	A7	A6	A5	A4

The following example illustrates switch selection corresponding to hex 2D0 (or binary 10 1101 xxxx). The "xxxx" represents address lines A3, A2, A1, and A0 used on the Card to select individual registers at the PPIs. See Chapter 6, Programming.

Hex Representation	2		D			
Conversion Multipliers	2	1	8	4	2	1
Binary Representation	1	0	1	1	0	1
Setup	OFF	ON	OFF	OFF	ON	OFF
Switch ID	A9	A8	A7	A6	A5	A4

Caution

Carefully review the address selection reference table on the previous page before selecting the card address. If the addresses of two circuits overlap you will experience unpredictable computer behavior.

Chapter 5: Software

ACCES supplies programs to support the IOD-48S Digital I/O card and, also, to help you develop your applications software. These programs are on CD that comes with your card and are as follows:

SETUP	This is a menu-driven, pictorial program to help you set the card address, interrupt level, change-of-state interrupt, and high level interrupt enable.
FINDBASE	Reports active and available address locations in your computer for assignment as the IOD-48S base address.
SAMPLE1.C	This program is under a directory titled CSAMPLES. It is a C-language software program that demonstrates how to program the change-of-state function.

SETUP

This program is supplied with the IOD-48S as a tool for you to use in configuring jumpers and switches on the card. It is menu-driven and provides pictures of the card on the computer monitor. You make simple keystrokes to select functions. The picture on the monitor then changes to show how the jumper or switches should be placed to effect your choices.

The setup program is a stand-alone program that can be run at any time. It does not require that the card be plugged into the computer for any part of the setup. The program is self-explanatory with operation instructions and on-line help.

Chapter 6: Programming

The IOD-48S is an I/O-mapped device that is easily configured from any language and any language can easily perform digital I/O through the card's ports. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing. However, a table could be used to convert the byte or word data ports to a logical reference.

Developing Your Application Software

If you wish to gain a better understanding of the programs, then the information in the following paragraphs will be of interest to you. Refer to the data sheets and 8255-5 specification in Appendix A.

A total of 16 address locations are used by the IOD-48S. The PPIs are addressed consecutively with Address bits A3 through A0 as follows:

Address	Port Assignment	Operation
Base Address	PA Group 0	Read/Write
Base Address +1	PB Group 0	Read/Write
Base Address +2	PC Group 0	Read Write
Base Address +3	Control Group 0	Write Only
Base Address +4	PA Group 1	Read/Write
Base Address +5	PB Group 1	Read/Write
Base Address +6	PC Group 1	Read/Write
Base Address +7	Control Group 1	Write Only
Base Address +8	Enable/Disable Buffer, Grp 0	Write Only
Base Address +9	Enable/Disable Buffer, Grp 1	Write Only
Base Address +B	Enable Chg-of-St. Interrupt	Write Only
Base Address +F	Clear Chg-of-St. Interrupt	Write Only

Table 6-1: Address Selection Table

The IOD-48S card uses two 8255-5 PPIs to provide a total of 48 bits input/output capability. The card is designed to use each of these PPIs in Mode 0 wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

Each PPI contains a Control Register. This write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each PPI should be configured during initialization by writing to the Control Registers even if the ports are only going to be used as inputs. Output buffers are automatically set by hardware according to the Control Register states. Note that Control Registers are located at base address +3 and base address +7. Bit assignments in each of these Control Registers are as follows:

Bit	Assignment	Code
D0 Bit	Port C Lo (C0-C3)	1=Input, 0=Output
D1	Port B	1=Input, 0=Output
D2	Mode Select	1=Mode 1, 0=Mode 0
D3	Port C Hi (C4-C7)	1=Input, 0=Output
D4	Port A	1=Input, 0=Output
D5, D6	Mode Select	00=Mode 0, 01=Mode 1, 1X=Mode 2
D7	Mode Set Flag	1=Active

Table 6-2: Control Register Bit Assignment

Note

Mode 1 and Mode 2 cannot be used by the IOD-48S without modification (Consult factory.). Thus, bits D2, D5, and D6 should always be set to "0" and (when the TST/BEN jumper is in the BEN position) Bit D7 to "1".

Note

In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer direction on this card. The control register should only be used for setting up input and output of the ports and enabling the buffer.

IOD-48S provides a means to enable/disable the tristate I/O buffers under program control. If the TST/BEN jumper on the card is installed in the BEN position, the I/O buffers are permanently enabled. However, if that jumper is in the TST position, enable/disable of the buffers is software controlled via the control register as follows:

The card is initialized in the receive mode by the computer reset command.

a. When bit D7 of the Control Register is set high, direction of the three ports of the associated PPI chip as well as the mode can be set. For example, a write to Base Address +3 with data bit D7 high programs port direction at Group 0 ports A, B, and C. If, for example, hex 80 is sent to Base Address +3, the Group 0 PPI will be configured in mode 0 with Ports A, B, and C as outputs.

b. At the same time, data bit D7 is also latched in a buffer controller for the associated PPI chip. A high state disables the buffers and, thus, all four buffers will be put in the tristate mode; i.e. disabled.

c. Now, if any of the ports are to be set as outputs, you may set the values to the respective port with the outputs still in the tristate condition. (If all ports are to be set as inputs, this step is not necessary.)

d. If data bit D7 is low when the control byte is written, ONLY the associated buffer controller is addressed. If, for example, a control byte of hex 80 has been sent as previously described, and the data to be output are correct, and it is now desired to open the three ports, then it is necessary to send a control byte of hex 00 to base address +3 to enable the Group 0 buffers. When you do this, the buffers will be enabled.

Note

Note that all data bits except D7 must be the same for the two control bytes.

Those buffers will now remain enabled until another control byte with data bit D7 high is sent to base address +3.

Similarly, the Group 1 ports can be enabled/disabled via the control register at base address +7. The following program fragment in C language illustrates the foregoing:

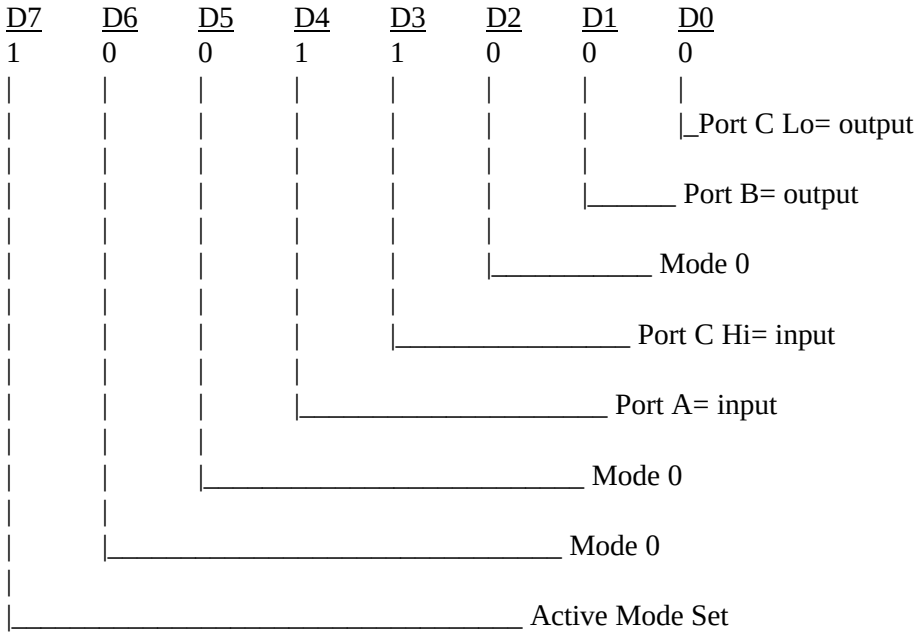
```
const BASE_ADDRESS 0x300;
outportb(BASE_ADDRESS +3, 0x89);      /*This instruction sets the mode to Mode 0, ports
                                       A and B as output, and port C as input. Since bit
                                       D7 is high, the output buffers are set to tristate
                                       condition. See item b. above.*/

outportb(BASE_ADDRESS,0);
outportb(BASE_ADDRESS+1,0);           /*These instructions set the initial state of ports A
                                       and B to all zeroes. Port C is not set because it is
                                       configured as an input. See item c. above.*/
 outportb(BASE_ADDRESS +3, 0x09);     /*Enable the tristate output buffers by using the
                                       same control byte used to configure the PPI, but
                                       now set bit D7 low. See item d. above.*/
```

Programming Example (Basic)

The following example in BASIC is provided as a guide to assist you in developing your working software. In this example, the card base address is 2D0 hex and the I/O lines of group 0 are to be setup as follows:

Port A = Input Port C Hi = Input
Port B = Output Port C Lo = Output

The first step is to configure the control register. Configure bits of the control register as:



This corresponds to 98 hex. If the card address is 2D0 hex, use the BASIC OUT command to write to the control register as follows:

```
10      BASEADDR=&H2D0
20      OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C:

```
30      X=INP(BASEADDR)          'Read Port A
40      Y=INP(BASEADDR+2)/16     'Read Port C Hi
```

To set outputs high (1) at Port B and the lower nybble of Port C:

```
50      OUT BASEADDR+1,&HFF      'Turn on all Port B bits
60      OUT BASEADDR+2,&HF       'Turn on all bits of Port C lower nybble
```

Enabling/ Disabling I/O Buffers

When using the tristate mode (Jumper in the TST position), the method to disable the I/O buffers involved writing a control word to the Control Register at Base Address +3 and Base Address +7. This control word was required to have bit D7 (the most significant bit) set.

That meant that the PPI translated it as an "active mode set" and reset the output data latches to "zero" on all output ports and the output buffers were disabled. However, if the buffers are to be enabled at a later time, the output latches will be in a "zero" state. For example, if all the outputs were 1's, they will now be 0's and the output buffers will be disabled. This problem can be resolved as follows.

Two computer I/O bus addresses are available that permit you to enable or disable the I/O buffers at will, without programming the PPI mode. Buffers for Goup 0 bits are enabled/disabled at Base Address +8 and buffers for Group 1 bits are enabled/disabled at Base Address +9. To enable the buffers and to set outputs to the desired state, you can write to the Control Register with bit D7 low. If you wish to subsequently disable the buffers, you can write to the Control Register with bit D7 high. In this way you can enable/disable the output buffers without programming the PPI mode.

Note

When writing a command byte to the IOD-48S while the TST jumper is installed, the PPI output buffers are disabled. Thus, when you desire to change the mode, you must first set the new mode and then enable the buffers. Enabling the buffers can be done at either Base Address +3 (or +7) or Base Address +8 (or +9).

Change-of-state Interrupts

At power-up or Reset, a register that enables change-of-state interrupts is set to zero. This enables all inputs to generate change-of-state interrupts. During initialization this register should be programmed to prevent interrupt generation by inputs that you do not want to cause change-of-state interrupts or by ports that are programmed as outputs. To program this Change-of-State-Interrupt-Enable Register, write to it at Base Address +B. Data bits D0 through D5 control ports A, B, and C of the 8255 PPIs as shown in Table 6-3.

Bit	Port Controlled
D0	Group 0, Port A
D1	Group 0, Port B
D2	Group 0, Port C
D3	Group 1, Port A
D4	Group 1, Port B
D5	Group 1, Port C

Table 6-3: Change-of-state-interrupt-enable Register

Writing a "one" disables the port; writing a "zero" enables it. This register is latched. To clear the latch, write anything at Base Address +F.

Sharing Interrupts on the ISA Bus

As noted on page 1-1, IOD-48S can facilitate an external interrupt via bit C3 at each 24-bit port. (The external interrupt is OR'ed with the change-of-state interrupt.) On occasion, however, a system application will require more interrupt levels than are available on the ISA bus. While this is not recommended, IRQ sharing is possible. Each card that is going to share an IRQ must strictly adhere to a special standard for accessing the IRQ lines as follows:

1. The interrupt must be held in a high impedance state until asserting an interrupt.
2. The interrupt must be asserted in the form of a low signal lasting at least 500 nanoseconds followed by a rising edge and then immediately returning to a high impedance condition.
3. The card must contain a status register or flag of some kind to indicate that it generated the interrupt. There is an exception to this rule. This is the case where only one card (of those sharing the interrupt level) does not provide a status bit to indicate that it asserted the interrupt but is otherwise capable of sharing the IRQ. In this case, it may share the interrupt level with other cards if (a) it is the only card on that IRQ level that does not have a status bit and (b) it is installed onto the IRQ vector first. (This makes it the last card to be called in the vector chain.) This scheme will work because it can be assumed that if every other card in the vector chain did not cause the interrupt, then the last card must be the one that did.

Note

Note that if two cards assert the IRQ line within 500 nanoseconds of each other, the second card in the ISR chain will not be serviced. It is possible to alleviate this problem by writing a single ISR that can detect the bit flag on every card and therefore detect the fact that two cards (or more) report generating an interrupt even though only one interrupt was processed by the CPU.

Chapter 7: Connector Pin Assignments

Two 50-pin headers are provided on the IOD-48S; one for each 24 I/O group. The mating connector is an AMP type 1-746285-0 or equivalent. Connector pin assignments are listed below. Notice that every second line is grounded to minimize crosstalk between signals.

Assignment		Pin		Assignment	Pin
Port C Hi	PC7	1		Ground	2
Port C Hi	PC6	3		Ground	4
Port C Hi	PC5	5		Ground	6
Port C Hi	PC4	7		Ground	8
Port C Lo	PC3*	9		Ground	10
Port C Lo	PC2	11		Ground	12
Port C Lo	PC1	13		Ground	14
Port C Lo	PC0	15		Ground	16
Port B	PB7	17		Ground	18
Port B	PB6	19		Ground	20
Port B	PB5	21		Ground	22
Port B	PB4	23		Ground	24
Port B	PB3	25		Ground	26
Port B	PB2	27		Ground	28
Port B	PB1	29		Ground	30
Port B	PB0	31		Ground	32
Port A	PA7	33		Ground	34
Port A	PA6	35		Ground	36
Port A	PA5	37		Ground	38
Port A	PA4	39		Ground	40
Port A	PA3	41		Ground	42
Port A	PA2	43		Ground	44
Port A	PA1	45		Ground	46
Port A	PA0	47		Ground	48
+5 VDC		49		Ground	50

Table 7-1: Connector Pin Assignments

* This line is an I/O port and also a User Interrupt.

Appendix A: Programmable Peripheral Interface Data Sheets

The data sheets in this Appendix are provided to help your understanding of the 8255-5 PPI which is made by a number of companies. These sheets are reprinted with permission of Mitsubishi Electric Corp. © 1987.

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Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesioproducts.com.***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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